



Patent Application for

5      **DIGITAL INTERFACE IN RADIO-FREQUENCY APPARATUS AND ASSOCIATED  
METHODS**

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**Cross-Reference to Related Applications**

15      This patent application claims priority to Provisional U.S. Patent Application Serial No.  
60/261,506, Attorney Docket No. SILA:072PZ1, filed on January 12, 2001. This patent  
application further claims priority to Provisional U.S. Patent Application Serial No.  
\_\_\_\_\_, Attorney Docket No. SILA:072PZ2, titled "Partitioned RF Apparatus with Digital  
Interface and Associated Methods," filed on March 2, 2001. This patent application incorporates by  
reference the above provisional patent applications in their entirety.

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Furthermore, this patent application relates to concurrently filed, commonly owned U.S.  
Patent Application Serial No. \_\_\_\_\_, Attorney Docket No. SILA:072, titled  
"Partitioned Radio-Frequency Apparatus and Associated Methods."

25      **Technical Field of the Invention**

This invention relates to radio-frequency (RF) receivers and transceivers. More  
particularly, the invention concerns (i) ways of partitioning high-performance RF receiver or

transceiver circuitry into circuit partitions so as to reduce interference effects among the circuit partitions, and (ii) circuits and protocols that facilitate interfacing among the circuit partitions.

## Background

5       The proliferation and popularity of mobile radio and telephony applications has led to market demand for communication systems with low cost, low power, and small form-factor radio-frequency (RF) transceivers. As a result, recent research has focused on providing monolithic transceivers using low-cost complementary metal-oxide semiconductor (CMOS) technology. Current research has focused on providing an RF transceiver within a single  
10 integrated circuit (IC). For discussions of the research efforts and the issues surrounding the integration of RF transceivers, see Jacques C. Rudell *et al.*, *Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems*, INVITED PAPER AT THE 1998 INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS, MONTEREY, CALIFORNIA; Asad A. Abidi, *CMOS Wireless Transceivers: The New Wave*, IEEE  
15 COMMUNICATIONS MAG., Aug. 1999, at 119; Jan Crols & Michael S. J. Steyaert, 45 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS – II: ANALOG AND DIGITAL SIGNAL PROCESSING 269 (1998); and Jacques C. Rudell *et al.*, *A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications*, 32 IEEE J. OF SOLID-STATE CIRCUITS 2071 (1997), all incorporated by reference here in their entireties.

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The integration of transceiver circuits is not a trivial problem, as it must take into account the requirements of the transceiver's circuitry and the communication standards governing the

transceiver's operation. From the perspective of the transceiver's circuitry, RF transceivers typically include sensitive components susceptible to noise and interference with one another and with external sources. Integrating the transceiver's circuitry into one integrated circuit would exacerbate interference among the various blocks of the transceiver's circuitry. Moreover, communication standards governing RF transceiver operation outline a set of requirements for noise, inter-modulation, blocking performance, output power, and spectral emission of the transceiver. Unfortunately, no method for addressing all of the above issues in high-performance RF receivers or transceivers, for example, RF transceivers used in cellular and telephony applications, has been developed. A need therefore exists for techniques of partitioning and integrating RF receivers or transceivers that would provide low-cost, low form-factor RF transceivers for high-performance applications, for example, in cellular handsets.

## Summary of the Invention

This invention provides interfacing techniques in radio-frequency (RF) apparatus, for example, receivers or transceivers. In one embodiment, an RF apparatus according to the invention includes receiver analog circuitry configured to produce a at least one digital receive  
5 signal from an analog radio-frequency signal. The receiver analog circuitry has a plurality of signal lines that are configurable by a control signal. The RF apparatus also has a receiver digital circuitry configured to accept the at least one digital receive signal from the receiver analog circuitry. The receiver digital circuitry has a plurality of signal lines that couple to the signal lines of the analog receiver circuitry. The signal lines of the digital receiver circuitry are also  
10 configurable by the control signal.

In another embodiment, a radio-frequency (RF) transceiver according to the invention includes a first integrated-circuit device that includes receiver analog circuitry configured to produce a at least one digital receive signal from an analog radio-frequency signal. The receiver  
15 analog circuitry has a plurality of signal lines that are configurable by a control signal. The RF transceiver also has a second integrated-circuit device that includes receiver digital circuitry configured to accept the at least one digital receive signal from the receiver analog circuitry. The receiver digital circuitry has a plurality of signal lines that couple to the signal lines of the receiver analog circuitry. The signal lines of the receiver digital circuitry are also configurable  
20 by the control signal.

Another aspect of the invention relates to methods of interfacing receiver digital circuitry and receiver analog circuitry within a radio-frequency (RF) apparatus, for example, a receiver or RF transceiver. In one embodiment, a method according to the invention includes providing receiver analog circuitry that has a plurality of signal lines that are configurable by a control  
5 signal. The method utilizes the receiver analog circuitry to produce at least one digital receive signal from an analog radio-frequency signal. The method also includes providing receiver digital circuitry that has a plurality of signal lines that are configurable by the control signal, and couple to the signal lines of the receiver analog circuitry. The method further includes accepting in the receiver digital circuitry the at least one digital receive signal from the receiver analog  
10 circuitry.

In another embodiment, a method according to the invention for interfacing receiver digital circuitry and receiver analog circuitry within an RF transceiver includes providing in a first integrated-circuit device a receiver analog circuitry that has a plurality of signal lines that are  
15 configurable by a control signal. The method further includes utilizing the receiver analog circuitry to produce at least one digital receive signal from an analog radio-frequency signal. The method provides in a second integrated-circuit device a receiver digital circuitry that has a plurality of signal lines that are configurable by the control signal and are coupled to the signal lines of the receiver analog circuitry. Finally, the method includes accepting in the receiver  
20 digital circuitry the at least one digital receive signal from the receiver analog circuitry.

## Description of the Drawings

The appended drawings illustrate only exemplary embodiments of the invention and therefore do not limit its scope. The disclosed inventive concepts lend themselves to other equally effective embodiments. In the drawings, the same numerals used in more than one  
5 drawing denote the same, similar, or equivalent functionality, components, or blocks.

FIG. 1 illustrates the block diagram of an RF transceiver. The RF transceiver includes radio circuitry that operations in conjunction with baseband processor circuitry.

10 FIG. 2A shows RF transceiver circuitry partitioned according to the invention.

FIG. 2B depicts another embodiment of RF transceiver circuitry partitioned according to the invention. In this embodiment, the reference generator resides within the same circuit partition, or circuit block, as does the receiver digital circuitry.

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FIG. 2C illustrates yet another embodiment of RF transceiver circuitry partitioned according to invention. In this embodiment, the reference generator circuitry resides within the baseband processor circuitry.

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FIG. 2D shows another embodiment of RF transceiver circuitry partitioned according to the invention. In this embodiment, the receiver digital circuitry resides within the baseband processor circuitry.

FIG. 3 illustrates interference mechanisms among the various blocks of an RF transceiver. The embodiments of the invention in FIGS. 2A-2D, depicting RF transceivers partitioned according to the invention, seek to overcome, reduce, or minimize those interference mechanisms.

FIG. 4 shows a more detailed block diagram of RF transceiver circuitry partitioned according to the invention.

FIG. 5 illustrates an alternative technique for partitioning RF transceiver circuitry.

FIG. 6 shows yet another alternative technique for partitioning RF transceiver circuitry.

FIG. 7 depicts a more detailed block diagram of RF transceiver circuitry partitioned according to the invention. In this embodiment, the receiver digital circuitry resides within the baseband processor circuitry.

FIG. 8 illustrates a more detailed block diagram of a multi-band RF transceiver circuitry partitioned according to the invention.

FIG. 9A shows a block diagram of an embodiment of the interface between the receiver digital circuitry and receiver analog circuitry in an RF transceiver according to the invention.

FIG. 9B depicts a block diagram of another embodiment of the interface between the baseband processor circuitry and the receiver analog circuitry in an RF transceiver according to the invention. In this embodiment, the receiver digital circuitry resides within the baseband processor circuitry.

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FIG. 10 illustrates a more detailed block diagram of the interface between the receiver analog circuitry and the receiver digital circuitry, with the interface configured as a serial interface.

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FIG. 11A shows a more detailed block diagram of an embodiment of the interface between the receiver analog circuitry and the receiver digital circuitry, with the interface configured as a data and clock signal interface.

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FIG. 11B illustrates a block diagram of an embodiment of a delay-cell circuitry that includes a clock driver circuitry in tandem with a clock receiver circuitry.

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FIG. 12 depicts a schematic diagram of an embodiment of a signal-driver circuitry used to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

FIG. 13 illustrates a schematic diagram of an embodiment of signal-receiver circuitry used to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

FIG. 14 shows a schematic diagram of another signal-driver circuitry that one may use to interface the receiver analog circuitry and the receiver digital circuitry according to the invention.

## 5 Detailed Description of the Invention

This invention in part contemplates partitioning RF apparatus so as to provide highly integrated, high-performance, low-cost, and low form-factor RF solutions. One may use RF apparatus according to the invention in high-performance communication systems. More particularly, the invention in part relates to partitioning RF receiver or transceiver circuitry in a way that minimizes, reduces, or overcomes interference effects among the various blocks of the RF receiver or transceiver, while simultaneously satisfying the requirements of the standards that govern RF receiver or transceiver performance. Those standards include the Global System for Mobile (GSM) communication, Personal Communication Services (PCS), Digital Cellular System (DCS), Enhanced Data for GSM Evolution (EDGE), and General Packet Radio Services (GPRS). RF receiver or transceiver circuitry partitioned according to the invention therefore overcomes interference effects that would be present in highly integrated RF receivers or transceivers while meeting the requirements of the governing standards at low cost and with a low form-factor. The description of the invention refers to circuit partition and circuit block interchangeably.

FIG. 1 shows the general block diagram of an RF transceiver circuitry 100 according to the invention. The RF transceiver circuitry 100 includes radio circuitry 110 that couples to an

antenna 130 via a bi-directional signal path 160. The radio circuitry 110 provides an RF transmit signal to the antenna 130 via the bi-directional signal path 160 when the transceiver is in transmit mode. When in the receive mode, the radio circuitry 110 receives an RF signal from the antenna 130 via the bi-directional signal path 160.

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The radio circuitry 110 also couples to a baseband processor circuitry 120. The baseband processor circuitry 120 may comprise a digital-signal processor (DSP). Alternatively, or in addition to the DSP, the baseband processor circuitry 120 may comprise other types of signal processor, as persons skilled in the art would understand. The radio circuitry 110 processes the  
10 RF signals received from the antenna 130 and provides receive signals 140 to the baseband processor circuitry 120. In addition, the radio circuitry 110 accepts transmit input signals 150 from the baseband processor 120 and provides the RF transmit signals to the antenna 130.

FIGS. 2A-2D show various embodiments of RF transceiver circuitry partitioned  
15 according to the invention. FIG. 3 and its accompanying description below make clear the considerations that lead to the partitioning of the RF transceiver circuitry as shown in FIGS. 2A-2D. FIG. 2A illustrates an embodiment 200A of an RF transceiver circuitry partitioned according to the invention. In addition to the elements described in connection with FIG. 1, the RF transceiver 200A includes antenna interface circuitry 202, receiver circuitry 210, transmitter  
20 circuitry 216, reference generator circuitry 218, and local oscillator (LO) circuitry 222.

The reference generator circuitry 218 produces a reference signal 220 and provides that signal to the local oscillator circuitry 222 and to receiver digital circuitry 212. The reference